Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.030”**

**.030”**

**Top Material: Al**

**Backside Material: Au**

**B = .0041” X .0043”**

**E = .004” X .0061”**

**Backside Potential: COLLECTOR**

**Mask Ref: 12**

**APPROVED BY: DK DIE SIZE .030” X .030” DATE: 7/7/22**

**MFG: Fairchild THICKNESS .007” P/N: MPSA06**

**DG 10.1.2**

#### Rev B, 7/19/02